Journal of Crystal Growth 383 (2013) 84–94

Contents lists available at ScienceDirect

Journal of Crystal Growth

journal homepage: www.elsevier.com/locate/jcrysgro

Optimization of a buffer layer for cubic silicon carbide growth on silicon substrates

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ARTICLE INFO

Article history:
Received 9 May 2013
Received in revised form
1 August 2013
Accepted 6 August 2013
Communicated by T. Paskova
Available online 23 August 2013

Keywords:
A1. Atomic force microscopy
A1. Characterization
A1. X-ray diffraction
A3. Chemical vapor deposition processes
A3. Hot wall epitaxy
B2. Semiconducting silicon compounds

ABSTRACT

A procedure for the optimization of a 3C–SiC buffer layer for the deposition of 3C–SiC/(001) Si is described. After a standard carbonization at 1125 °C, SiH_4 and C_3H_8 were added to the gas phase while the temperature was raised from 1125 °C to the growth temperature of 1380 °C with a controlled temperature ramp to grow a thin SiC layer. The quality and the crystallinity of the buffer layer and the presence of voids at the SiC/Si interface are related to the gas flow and to the heating ramp rate. In order to improve the buffer quality the SiH_4 and C_3H_8 flows were changed during the heating ramp. On the optimized buffer no voids were detected and a high-quality 1.5 μm 3C–SiC was grown to demonstrate the effectiveness of the described buffer.

1. Introduction

Cubic silicon carbide (3C–SiC) is an interesting wide-bandgap material for applications in high power electronic devices working at high frequency, high temperature, harsh environments, and for micro-electro-mechanical systems (MEMS) [1]. Its biocompatibility makes it an ideal candidate for MEMS working in the human body [2] while its high breakdown electric field strength (1–3 MV/cm) is the most important factor for its use in high power applications [3]. When employed in high-frequency devices the saturated electron drift velocity of SiC ($2–2.5 \times 10^7$ cm/s) is twice the one of silicon, thus enabling microwave devices to reach high channel currents [4]. Thanks to its lattice parameter it is an ideal substrate for the heteroepitaxial growth of nitride compound semiconductors and it is also largely used for the epitaxial deposition of graphene, although in this case an atomically flat surface is needed, often obtained through a dedicate preparation via high temperature hydrogen etching procedures [5].

4H and 6H–SiC wafers are nowadays available in sizes up to 4″ with 6″ prototypes in development. However, due to the very high cost of 4H and 6H substrates, 3C–SiC is also alternatively considered because it has one of the largest electron mobilities ($800\ cm^2\ V^{-1}\ s^{-1}$) and saturated drift velocities (2.5×10^7 cm/s) of all polytypes despite its smallest bandgap. Due to the difficulties in growing bulk crystals, 3C–SiC is usually heteroepitaxially grown on silicon substrates thus exploiting advantages in low-cost large-size wafers and the possibility to fabricate MEMS using the well-developed Si microfabrication technology [6].

Unfortunately, due to the large lattice mismatch of about 20% and to the difference in thermal expansion coefficients, SiC/Si heteroepitaxy is still problematic and a lot of work has been devoted to the deposition of 3C–SiC using different deposition techniques, precursors temperature ranges, and growth recipes [7–12]. Despite all these efforts important issues such as poor crystal quality, surface roughness, residual stress, and wafer bending still prevent the widespread realization of 3C–SiC devices and applications [13–15].

The first breakthrough in the deposition of 3C–SiC/Si have been achieved by Nishino et al. [16] in 1983, with the development of the carbonization process. In many growth processes propane and H_2 are usually introduced at temperature lower than the one of

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http://dx.doi.org/10.1016/j.jcrysgro.2013.08.005

film growth, to convert Si surface into SiC. Then the temperature is increased and a thick 3C–SiC layer is grown using SiH_4 and C_3H_8.

In order to obtain 3C–SiC layers with high crystallinity, flat surface, and low defect density the growth temperature is usually close to the silicon melting point (1414 °C). The standard 3C–SiC deposition processes are carried out at about 1350–1380 °C [1]. Lower deposition temperatures (1000–1200 °C) are also employed but the resulting film, even if it is suitable for MEMS realization, generally has poorer crystal quality and rough surfaces and may not be suitable for advanced (bio)sensor devices or graphene synthesis, which requires a very flat and perfect surface.

In addition to standard or improved carbonization processes, several multistep methods were investigated, with different heating ramp rates or introduction of silane and propane in variable concentration between the carbonization step and the growth itself [7,11,12,17,18]. All these procedures consist actually in the deposition of a "low-temperature" SiC buffer layer often 10–200 nm thick after the carbonization step (which is normally just some nm thick) and before the thick 3C–SiC layer is grown in the 1350–1380 °C temperature range. The deposition of low temperature buffer layers is of widespread use in lattice mismatched epitaxy (e.g. GaN/sapphire, Ge/Si, InGaAs/InP) and is commonly used to relieve lattice mismatch to reduce strain and to increase the quality of the thick epitaxial layer [19]. 3C–SiC growth is still characterized by a large number of defects and high strain, and one of the key-points to obtain high quality and low stress material for devices and applications is to optimize the buffer layer. 3C–SiC literature is still lacking an in-depth description of the procedures to optimize the buffer layer deposited between the carbonization and the thick film. While some papers give some of these growth details[20–22], a lot of studies just report a generic addition of silane and propane during the heating up ramp without specifying the Si/C ratio, ramp heating rates, discussing the buffer quality or its impact on the high temperature film growth.

In this paper we will report a detailed optimization procedure for the deposition of a low temperature 3C–SiC buffer layer, with extensive characterization of the first 100–150 nm low temperature 3C–SiC growth. On the top of this buffer layer we were able to deposit a high quality 3C–SiC with high crystallinity and low stress. The resulting films were comparable to the state of the art, and we would like to stress the importance of understanding the relation between the buffer layer deposition process and the subsequent thick film growth: without an appropriate optimization of the buffer layer, high quality SiC films could not be obtained. Thus, a deeper understanding of a low temperature SiC buffer deposition is very important for future development of SiC/Si heteroepitaxy.

2. Experimental

The SiC films were grown in a home made horizontal hot wall reactor heated by radio frequency. Standard silane and propane (both 3% diluted in H_2) were used as reagents while palladium purified H_2 was used as carrier gas. The growth was performed on (001) silicon substrates cut in chips about 2×4 cm^2, etched in 1:10 HF:H_2O for 60 s before being inserted in the growth chamber.

The carbonization step was optimized by flowing a mixture of 4000 sccm of H_2 and 200 sccm of C_3H_8 during a 20 min linear heating ramp rate from RT to 1125 °C. The pressure was set at 700 mbar for the entire duration of the ramp and once reached 1125 °C the temperature was held constant for 5 min to complete the carbonization step.

After the carbonization the pressure of the growth chamber was reduced to 200 mbar in order to reduce the tendency of silicon to react in the gas phase and to form precipitates. We focused our analysis on the growth optimization of the buffer layer: the basic idea was to deposit a thin SiC layer (100–150 nm) using SiH_4 and C_3H_8 while the temperature increased from 1125 °C to the actual (fixed) growth temperature of 1380 °C. Different procedures were tested: several heating rates were used from 1125 °C to 1380 °C and the SiH_4 and C_3H_8 flows was kept constant or changed abruptly during the ramp when a particular temperature was reached, as will be explained in the discussion.

In order to investigate the buffer quality and its development during the heating ramp we stopped the growth at selected temperatures during the heating from 1125 to 1380 °C: we fixed these analysis points at 1240 °C and 1280 °C. Moreover, the quality of the complete buffer was investigated by stopping the experiment at 1380 °C just before growing the SiC film.

In order to evaluate the impact of the buffer on the film we deposited a SiC layer for 30 min at 1380 °C and 200 mbar, with Si/C = 1.4.

The layers surface was analyzed by Atomic Force Microscopy (AFM) in contact mode by using a Digital Instruments Nanoscope IIIa. Usually, a first visual inspection by the naked eye was sufficient to observe a hazy/milky surface indicating a rough or imperfect surface due to non-optimal parameters chosen for the growth. The growths (both of buffer layers and thick films) with good characterization results (as by XRD, SEM, TEM) were always extremely mirrorlike.

Transmission Electron Microscopy (TEM) images were acquired using a Field Emission Gun (FEG) TEM/STEM JEOL 2200FS microscope operated at 200 kV. Images were acquired in the TEM two beam diffraction contrast and high resolution (HR-TEM) modes as well as in the STEM mode with a High Angle Annular Dark Field (HAADF) detector. ⟨110⟩ cross section specimens for TEM were prepared by sandwiching a piece of sample between two slabs of Si. The sandwich was then mechanically ground down to 30–40 μm and subsequently thinned to electron transparency by Ar ion beam bombardment.

Scanning Electron Microscopy (SEM) investigations were carried out with an FEG JEOL 6400F instrument at a beam energy of 4 keV.

Raman spectra were collected in backscattering depolarized geometry with a long focal 50× objective, using a JobinYvon T64000 spectrometer in single monochromator mode (employing a 1800 grating/mm grating, with a typical resolution < 4 cm^{-1}) and laser at 488 nm with maximum power to the sample < 1 mW. Typical integration times ranged from 10 to 60 s. For the data analysis, given the presence of an important Si background signal, particularly in the region of the second order Si phonon mode around 970 cm^{-1}, we modeled a Si background spectrum by spline interpolation, and this was subtracted as a background of fitted amplitude from each spectrum in the fitting procedure (see the supporting informations for more details). Raman peak shape was then represented as a pseudo-Voigt shape.

X-ray photoemission spectroscopy (XPS) was performed ex-situ in a UHV apparatus for surface electron spectroscopy. The Mg-K_α emission at 1253.6 eV is used as X-ray source while the photoelectrons are analyzed by a PSP electron energy analyzer, leading to a total energy resolution of 0.85 eV. Spectra are performed at low (Pass Energy = 50 eV) and high (PE = 10 eV) resolution to achieve wide range spectra and the C 1s, Si 2p core levels analysis. Lineshape analysis has been performed by subtracting a Shirley background and then applying Voigt lineshape with Lorentzian to Gaussian ratio of 0.3. X-ray Photoelectron Diffraction (XPD) has been performed at fixed azimuthal angle and variable polar angle on the bulk samples at low resolution (PE = 20 eV), to investigate the presence of ordered structure in the films. In order to remove air contaminants, samples were cleaned in an ultrasonic bath of trichloroethylene, acetone and final isopropyl alcohol before the

introduction into the analysis chamber, then outgassed in UHV (at 250 °C).

X-Ray Diffraction (XRD) spectra and the mosaic spread of the SiC film were collected using a custom modified Philips X-Ray diffractometer using Cu K_α radiation (8.04 keV) and a Göbel mirror to investigate the (002) reflection of SiC.

3. Results and discussion

3.1. Carbonization

Before studying the role of the buffer layer on the quality of the SiC film, the first step was to verify that the carbonization procedure could grant optimal results. Since the optimization of the carbonization step is not the primary focus of this work we do not discuss here the results of the different procedures we tested, and we do not want to study how the variation of the different growth parameters (ramp time, flow temperature, temperature of C_3H_8 injection etc.) affects the properties of the carbonization layer. The result of our carbonization procedure was a macroscopically mirrorlike surface and TEM analysis (Fig. 1) shows that Si substrate was actually converted in SiC with a thickness of 4–5 nm. The Selected Area Electron Diffraction (SAED) pattern clearly shows the diffraction spots of SiC and it is important to emphasize the fact that the SiC layer is smooth, densely packed, and no holes/pits were evidenced at the SiC/Si interface. XPS analysis (Fig. S1, S2, Table S1) confirmed the uniform carbonization of the whole substrate. This carbonization procedure was selected as a standard template for the growth of a thicker SiC film and was used as a starting point for all the subsequent depositions.

3.2. Optimization of the low temperature buffer layer for 3C–SiC growth

The first experiments were performed without the deposition of any buffer layer between the carbonization and the thick SiC film. After the carbonization process the pressure was lowered to 200 mbar and a fast heating ramp (3–4 min) was used to raise the temperature from the carbonization (1125 °C) to the film growth (1380 °C), without injecting any reagent. At 1380 °C the SiC film was deposited using 4000 sccm H_2 but although several Si/C ratios were tried ranging from 0.6 to 1.6 the resulting film was macroscopically hazy, with a milky, not mirrorlike surface. This first naked eye observation was sufficient to evidence several problems in the growth and the non-optimization of the recipe parameter. The XRD spectra of these films always showed only the (111) peak indicating that the resulting film was not epitaxial with substrate.

In order to avoid this problem, the buffer was introduced as an intermediate layer between the carbonization and the SiC film. SiH_4 and C_3H_8 were injected in the growth chamber during the heating ramp with Si/C=1. In order to analyze the growth progress we decided to analyze the deposition results by stopping the growth at intermediate temperatures between the carbonization and the growth temperature. The first analysis step was chosen at 1240 °C but we observed that, by using the fast heating ramp described previously, the film surface was still milky and not mirrorlike even when the growth was stopped at 1240 °C.

The samples were observed in cross section with SEM and a very high density of holes and pits was found at the interface between SiC and Si, as usually reported in literature [23]. Voids such as the ones in our films are typically attributed to the silicon outdiffusion from the substrate, promoted by non uniform SiC deposition. A non-optimal coalescence between SiC islands or mutual misorientation of micro-crystallites nucleated on the carbonized Si, could act as preferential channels for Si evaporation from the surface, thus forming pits in the substrate [24].

In order to overcome this problem a slower heating ramp from 1125 °C to 1380 °C was used. The basic idea was to deposit a compact SiC layer at low temperature in order to "seal" the Si below a thin uniform and epitaxial SiC film. In this way, even when the temperature is high enough to provide energy to the Si substrate atoms to outdiffuse, there would be less preferential ways to reach the surface (lower density of grain boundaries, uncovered areas etc.). Deposition of a low temperature layer in lattice mismatched heteroepitaxy is also often used to relax the strain with the controlled generation of defects, that usually remain confined in the buffer [19].

Two different heating ramps from 1125 °C to 1380 °C (21.5 °C/min and 25.5 °C/min) and two different SiH_4–C_3H_8 flows always with Si/C=1 (17–6 sccm and 27–9 sccm for SiH_4–C_3H_8 respectively) were tested. We will refer to these conditions as "slow/fast" ramp and "low/high" flow regime, respectively.

By stopping the growth at 1240 °C we observed a significant macroscopical enhancement of the sample quality. In the best cases (slow ramp with both low and high flows) the haziness previously observed by naked eye completely disappeared.

Fig. 2 shows the surface analysis by AFM of four samples grown under different conditions after stopping the growth at 1240 °C. Higher flow regimes promote the nucleation of smaller grains and

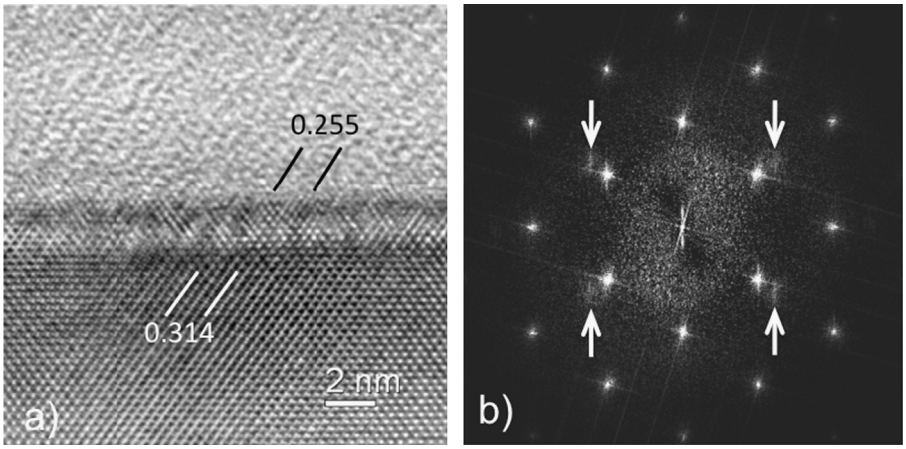

Fig. 1. (a) Wiener-filtered HR-TEM ⟨110⟩ cross section image of a carbonized silicon substrate and (b) corresponding Fast Fourier Transform showing its reciprocal lattice. In (a) the distance between the inclined planes in the top 2 nm is 0.255 nm, which is the lattice spacing of the SiC (111) planes. Six of such planes are located between the two black segments. The {111} lattice spacing of Si is 0.314 nm, as indicated in white. The diffraction pattern shown in (b), where the weak {111} Bragg spots of SiC are indicated by arrows, confirms the formation of a carbonized layer.

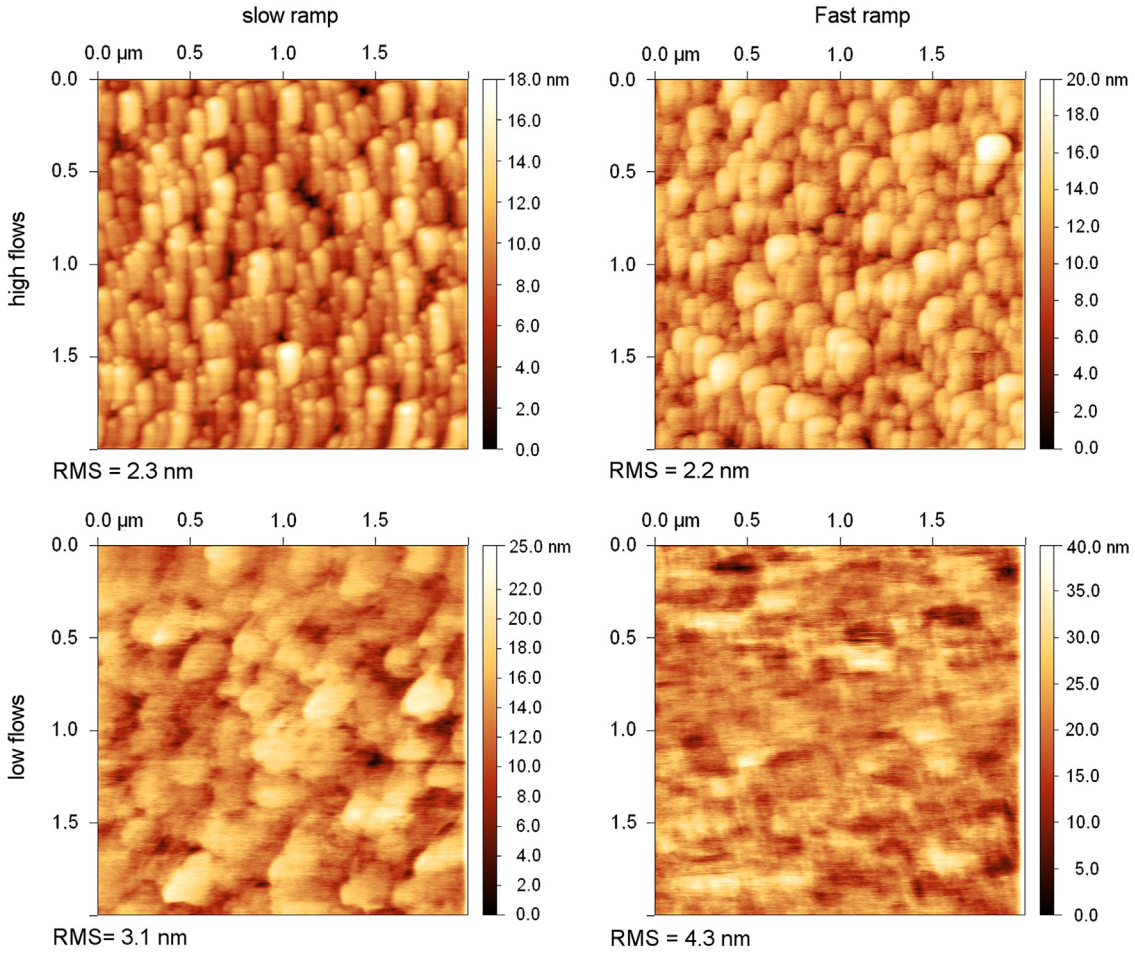

Fig. 2. AFM images of the SiC buffer layer at 1240 °C grown in different conditions. Note that the scale is different for each sample, in order to enhance the contrast.

islands with dimensions of about 200–300 nm while lower flows increase the surface roughness and result in larger grains. In all the cases the AFM images suggest a nucleation and growth mechanism typical of largely mismatched heteroepitaxial systems, namely Stranksy–Krastanov or Volmer–Weber. Even if the carbonization layer is smooth and with no evidence of islands, the strain generated by the lattice mismatch is still not relieved and the 2D growth mechanism known as Frank–Van Der Merwe is not observed.

Macroscopically, only the samples grown with the slower ramp with either high or low flows showed a mirrorlike surface, while the ones grown with the fast ramp appear slightly hazy and milky.

After the first analysis of the buffer at 1240 °C, the flows and heating ramp used for the first buffer step were kept constant in order to deposit a complete buffer, stopping the growth at 1380 °C just before starting the film deposition. Again, we observed a degradation of the surface morphology, that appeared hazy and milky regardless of the growth conditions adopted.

The reason for this behavior could be understood by considering that an increase of the temperature results in enhanced precursor cracking at the reactor inlet, leading to faster reaction and depletion of both SiH_4 and C_3H_8 in the gas phase. Depending on the growth chamber design and on flowdynamic/chemical kinetics of the system, this may decrease significantly the precursors partial pressure on the substrate downstream the chamber, leading to a growth rate reduction. In order to maintain a sufficient precursor overpressure to grow a high quality SiC buffer we increased the flows when temperature reached 1240 °C, after the deposition of the first step of the buffer, according to Table 1.

Table 1
SiH_4 and C_3H_8 flows used for the deposition of the SiC buffer layer.

(Flows in sccm)	First buffer step from 1125 to 1240 °C		Second buffer step from 1240 to 1280 °C		Third buffer step from 1280 to 1380 °C	
	SiH_4 flow	C_3H_8 flow	SiH_4 flow	C_3H_8 flow	SiH_4 flow	C_3H_8 flow
Low flows	17	6	34	12	51	18
High flows	27	9	48	16	72	24
H_2 carrier	1600		2500		3300	

Along the increase of the precursor gases, also the H_2 carrier gas flow was raised, resulting in higher gas velocity and faster transport of the precursor over the substrate, to compensate the effect of the higher cracking efficiency in the upstream region of the growth chamber. Another reason for surface roughening may also be ascribed to the increased adatom mobility due to temperature increase [25].

To analyze this second step of the buffer growth sequence we stopped the growth at 1280 °C and observed the results. By using a fast ramp, regardless of the flow rate we still observed a macroscopically hazy and milky surface while it became far better with the slow ramp with both high and low flows rate.

Following the same idea that lead to increase the flows from 1240 °C to 1280 °C, the flows were increased again, according to Table 1 for the deposition of the third buffer step, when temperature reached 1280 °C to compensate the enhanced cracking, until the end of the buffer deposition at 1380 °C.

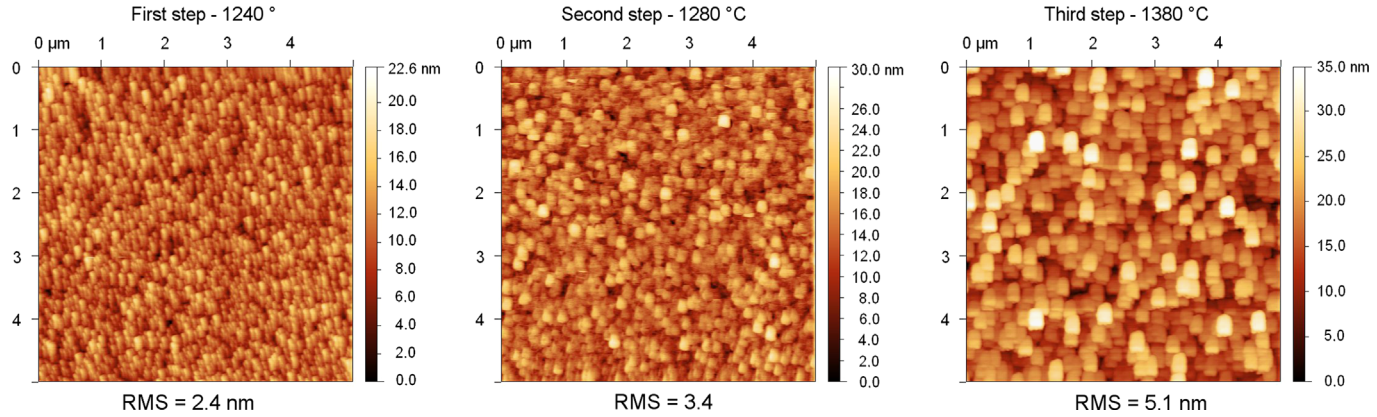

Fig. 3. Evolution of the buffer layer using the slow ramp rate and high flows regime.

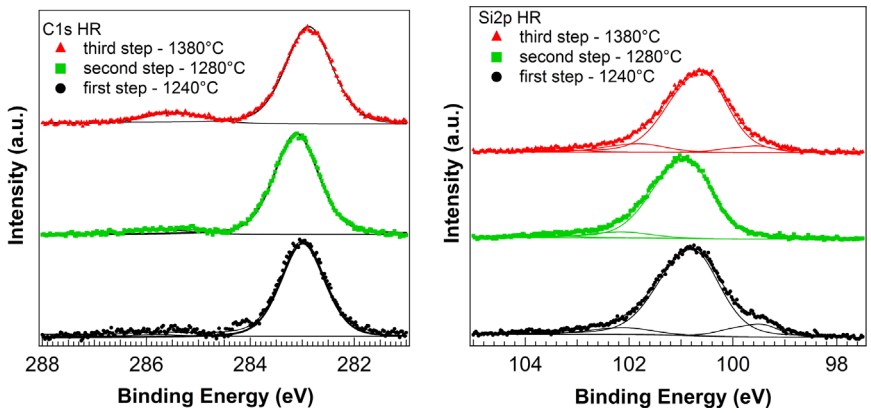

Fig. 4. High resolution XPS spectra of three buffer layers at PE=10 eV, background subtracted and with lineshape analysis. Left: C 1s. Right: Si 2p.

By using the slow ramp we obtained a mirrorlike buffer surface both with the high and low flows rate regimes, while non-optimal results were obtained with the fast ramp, regardless of the flows. As an example, Fig. 3 shows the evolution of the three steps of the buffer layer by using the high flows regime. It is interesting to observe that the islands nucleated in the first buffer step undergo a progressive enlargement during the subsequent steps, resulting at 1380 °C in well definite square plateaus about 200 nm wide, with almost flat top surface.

XPS wide range spectra (Fig. S1) show the different chemical species on the surface, in particular silicon and carbon and some oxygen, suggesting a slight surface oxidation as expected in ex-situ analysis. XPS spectra of C 1s core level (Fig. 4) put in evidence the presence of a main component in the 283–283.3 eV binding energy (BE) range for all growth steps, slightly shifted with respect to the expected value of 282.5 eV of cubic 3C–SiC [26]. Si 2p main component is located at about 100.8–101 eV, showing the same BE shift of the C 1s core level.

The very low Full Width at Half Maximum (FWHM) of the main C 1s component (~1.0 eV), and the C 1s to Si 2p BE distance of 182.3 eV suggest the presence of very crystalline films, being these values typical of 3C–SiC [27]. The observed BE shift at the different growth steps can be thus related to a band bending effect.

In order to understand the reasons for the degradation of the buffer layer using the different growth processes, 4 complete buffer layers were deposited by combining the high/low flows with the fast/slow ramp, stopping the process at 1380 °C just before the film deposition to analyze the results (Table 2).

Fig. 5 shows the SEM cross section of the four samples and the optical microscope image of 2 selected buffers, evidencing rougher surface and a high density of interface pits and voids for the samples grown with the fast ramp. The mesoscale microscope images clearly show the drastic reduction of interfacial voids occurring for sample C grown with the slow ramp.

Table 2
Labels for the different buffer layers realized by stopping the growth at 1380 °C. The corresponding approximate growth rate is indicated in parentheses.

	Low flow rate	High flow rate
Fast T ramp (25.5 °C/min)	A (18 nm/min)	D (15 nm/min)
Slow T ramp (21.5 °C/min)	C (6 nm/min)	B (5 nm/min)

The samples grown with low flows+fast ramp (sample A) and with high flows+slow ramp (sample B) were also analyzed by TEM (Fig. 6). The differences between the two samples are remarkable: while sample A shows high degree of polycrystallinity, high density of interface pits/voids (some with sizes up to 100–200 nm as shown in the SEM image of Fig. 5)-, rough surface and a structure composed mainly of misoriented grains, sample B appears perfectly (001) oriented, with smooth surface consisting mainly of plateau 200–300 nm wide and stacking defects, like stacking faults and twins. Very few voids and pits were observed at the interface. TEM images of sample B confirm also the shape and the flat top of the plateaus observed by AFM. XRD spectra on samples A and B confirm the crystallinity results found by TEM.

Fig. 7 shows the comparison between these two samples and sample C, grown with slow ramp+low flows regime. Sample A shows a single (111) peak, while it is remarkable that for samples B and C a single (002) peak is found, indicating that these samples

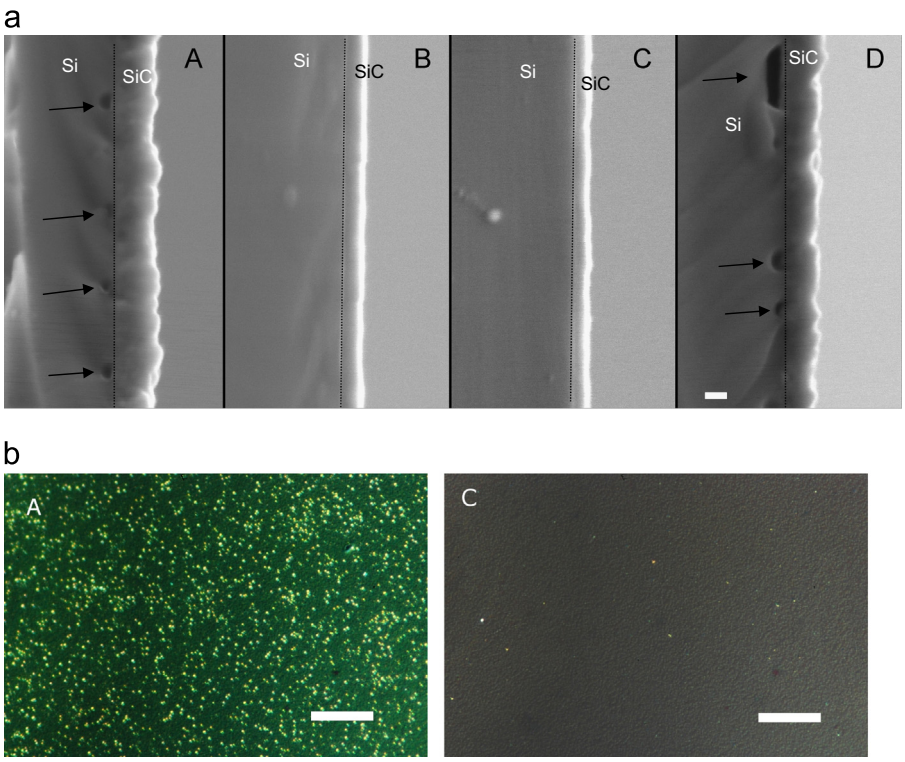

Fig. 5. (a) SEM cross section images of SiC buffers grown under different conditions. The interface is indicated by a dotted line and the pits at the SiC/Si interface are indicated by arrows. (A) low flows+fast ramp (about 180 nm thick), (B) high flows+slow ramp (about 60 nm thick), (C) low flows+slow ramp (about 70 nm thick) and (D) high flows+fast ramp (about 150 nm thick). The marker is indicated in sample D and is 100 nm for all the images. (b) Optical microscope images of buffers A and C. Markers in the photos are 50 μm.

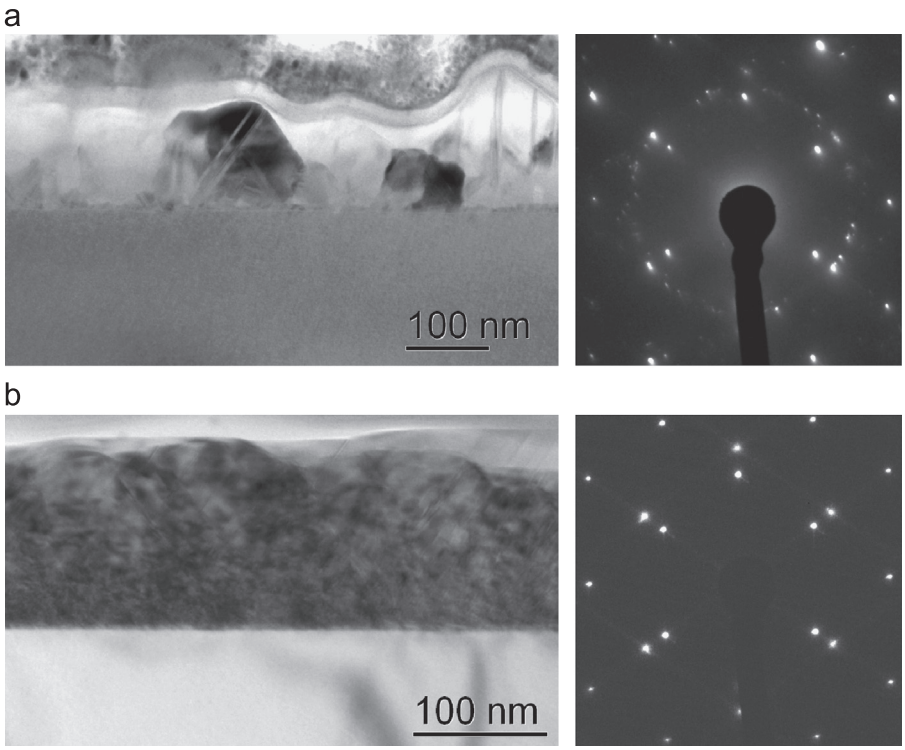

Fig. 6. TEM images of third step buffer layers grown combining (a) low flows with fast ramp (sample A) and (b) high flows with slow ramp (sample B). Left panels are the TEM diffraction contrast images, while the corresponding SAED patterns are reported on the right panels. In the latter ones the diffraction spots of Si are also visible as the SAED aperture also included the Si substrate.

are in a good epitaxial relation with the (001) Si substrate. The (FWHM for samples B and C is, respectively, about 1400" and 1800″, indicating that the growth with high flows regime results in a better crystallinity. No significant difference in terms of surface morphology and surface roughness were observed by AFM for samples B and C.

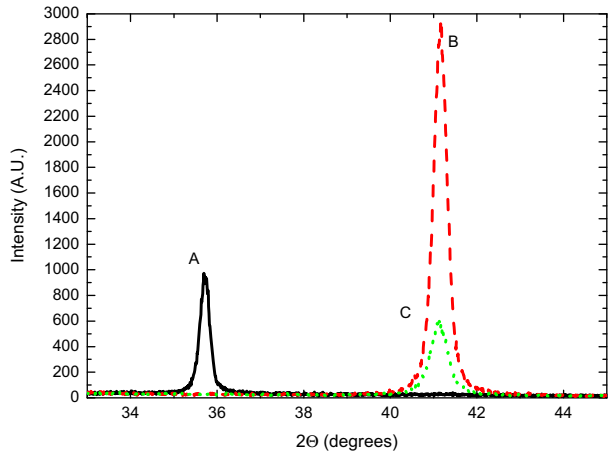

Fig. 7. XRD spectra of buffer layers grown by combining low flows rate with fast ramp (A), high flows rate with slow ramp (B) and low flows rate with slow ramp (C).

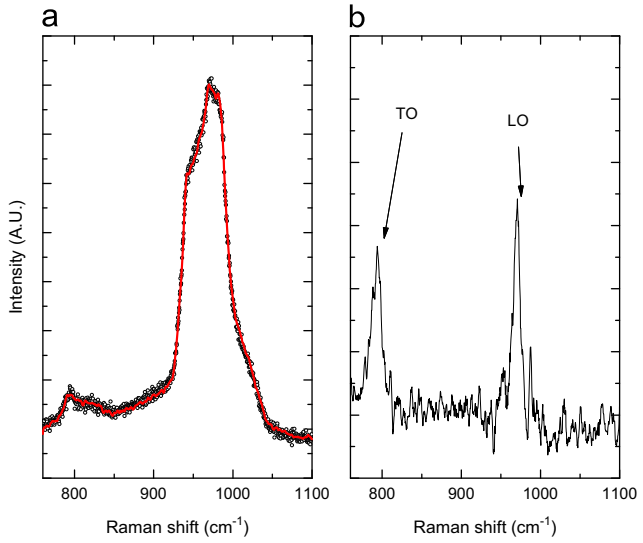

Fig. 8. Raman spectrum acquired on sample B, grown with high flows+slow ramp: (a) the experimental points (open dots) were fitted (solid line) and the SiC data (b) are presented after removal of the silicon background according to the procedure explained in Section 2.

Raman spectroscopy (Fig. 8) was used to get a detailed analysis of the crystalline quality and residual strain for the step 3 – sample B – of the buffer layer, and to compare them with the results on the SiC film grown on the buffer, discussed later.

After removal of the silicon background from the experimental data (Fig. 8b) the allowed LO peak is observed at about 970 cm^{-1} while the observation of a Raman TO peak at 792.7 cm^{-1} should be forbidden in our geometry: its presence can only be related to poor crystallinity, that is not surprising considering the high density of defects observed by TEM and the large FWHM of the XRD peak [28]. It is known that Raman peak position is very sensitive to the residual strain. The TO and LO peaks shift in dependence of the lattice mismatch $\Delta a/a$ due to stress according to a linear relation [29]:

$$\omega_{TO} = 796.5 - (3734 \pm 30)\Delta a/a$$

$$\omega_{LO} = 973 - (4532 \pm 30)\Delta a/a$$

Considering the TO peak position at 792.7cm^{-1} we can estimate a tensile lattice strain $\Delta a/a$ in the buffer of about 0.1%. A similar behavior is expected also for the LO peak position, however in this case a precise quantification of the strain is difficult because of the coincidence, in the same spectral region, of the second order Si phonon mode that lead to uncertainty in the correct determination of the peak position and for the doping dependence of this phonon mode. Despite very accurate modeling of the data, this makes an accurate evaluation of the shift particularly difficult in the LO case.

3.3. Growth of thick 3C–SiC film on optimized low temperature buffer layer

Following these analysis, buffer B was considered as the best template for subsequent SiC thick film growth. A SiC layer was thus deposited using the procedure described for the growth of buffer B and by growing the SiC layer immediately after the deposition of the buffer at 1380 °C and 200 mbar, for 30 min with Si/C = 1.4.

The film appears mirrorlike by naked eye and the AFM analysis (Fig. 9) reveals a very smooth surface with typical anti phase domains usually observed in literature due to the growth on a perfectly oriented (001) Si substrate [30].

Higher resolution AFM images (Fig. S3) show the presence of surface steps with a height corresponding approximately to the SiC lattice parameter, suggesting a highly uniform and ordered step-flow growth. The Root Mean Square (RMS) surface roughness measured on an area of $5 \times 5\ \mu m^2$ and averaged on several images is about

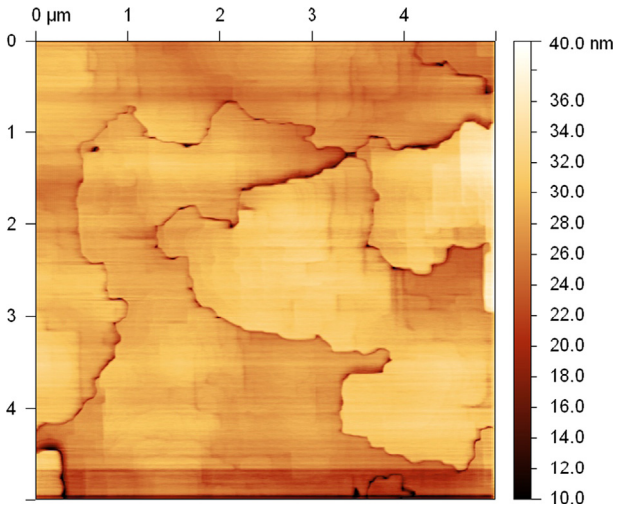

Fig. 9. AFM analysis of the thick SiC layer grown on buffer B.

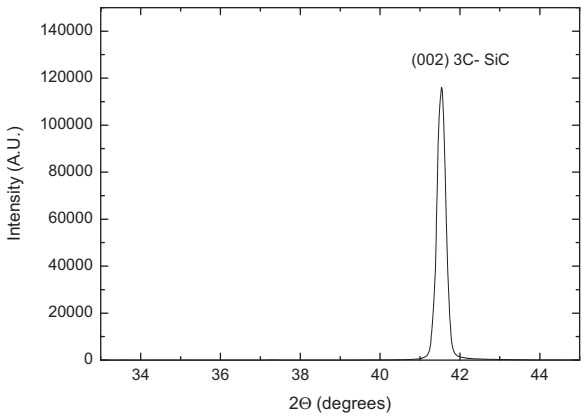

Fig. 10. XRD spectra of the SiC layer grown on optimized buffer layer.

2 nm, while on a $1 \times 1\ \mu m^2$ area is below 1 nm. It is interesting to observe the absence of the small islands observed by AFM in the complete buffer (third step of Fig. 3), which have evolved into large plateaus. The surface roughness of the SiC film is also lower than the buffer one. This growth behavior is typical of heteroepitaxial systems such e.g. GaN/sapphire or AlN/sapphire in which, after the low temperature buffer layer, islands with mutual misorientation grow at different rate and the fast-growing ones coalesce to form larger domains [31].

XRD spectra (Fig. 10) shows the presence of a very intense (002) 3C–SiC peak at 41.5° with FWHM of about 790″, indicating a high quality monocrystalline film. No evidence of (111) 3C–SiC peak was found. Considering the thickness of this film (about 1.5 μm), the observed FWHM is very small [32]. The reciprocal lattice map of the SiC film around the (002) node of SiC (Fig. 11) was obtained to understand the mosaic spread of the layer (vertical section of the peak). The measured value of about 0.3° is a further indication of good crystalline quality and corresponds to a very low misorientation of the mosaic domains with respect to the (001) direction.

Fig. 12 shows a typical TEM image of the SiC layer. A "standard" SiC structure is evidenced, with a high density of stacking defects typical of this heterosystem and due to the high lattice mismatch between SiC and Si combined with the very low formation energy of stacking faults and twins in SiC [33]. As observed by the SAED spectra and TEM images near the surface (Fig. 12b) the density of the stacking defects reduces significantly by moving towards the surface.

After removal of the silicon background from the experimental data (Fig. 13b) the Raman spectrum obtained on the SiC film shows an intense LO peak at 970.8 cm^{-1} with FWHM=4.4 cm^{-1} and a TO peak at 795.3 cm^{-1} with FWHM=6 cm^{-1}. It is interesting to compare the intensity of the peaks in the film (Fig. 13) with the one observed in the buffer (Fig. 8). The integrated intensity of the LO peak is expected to increase by increasing the crystallinity of the 3C–SiC layer due to the selection rule for the (001) surface of zinc-blende crystal, since the TO mode is forbidden while the LO mode is allowed [28].

This behavior is actually observed in our samples, considering that for the buffer we had LO/TO ratio of about 2, while in the film the LO/TO ratio increases to 12. A study of correlation between TO line width and intensity ratio TO/LO as reported in [34] could be interesting; unfortunately in our case, basing on two points only, no significant trend could be extrapolated. This could be however an interesting topic for a future study. This result confirms the good crystallinity of the film and the improvement of crystal quality going from the buffer to the film. Also the FWHM of the TO peak decreases from 18 cm^{-1} in the buffer to about 6 cm^{-1} in the

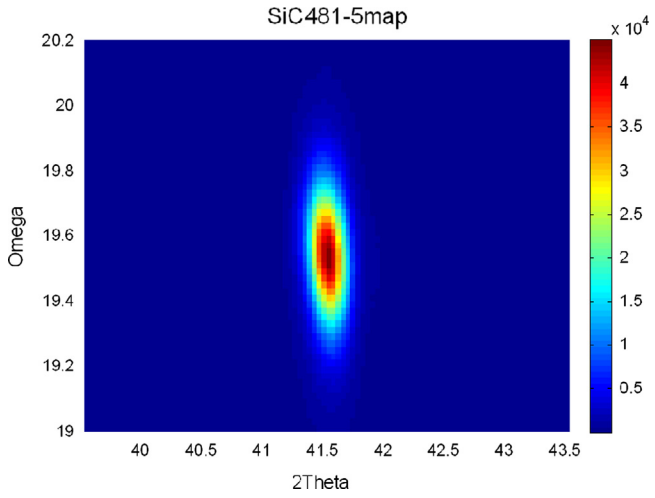

Fig. 11. Reciprocal lattice map near the 002 node of SiC.

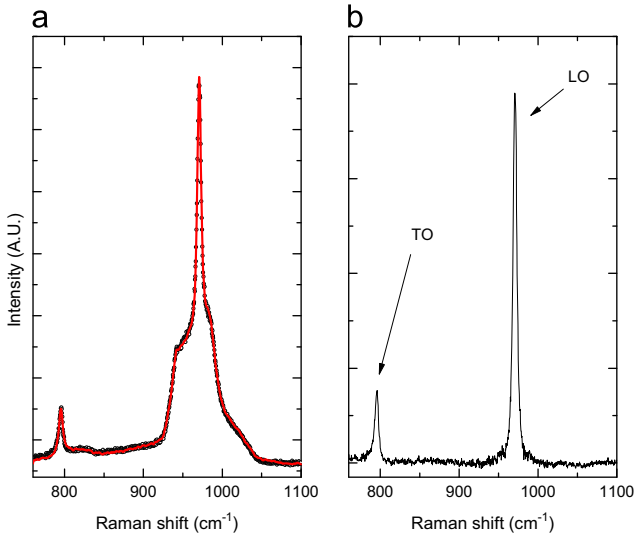

Fig. 13. Raman spectrum of the thick SiC film grown on buffer B: (a) the experimental points (open dots) were fitted (solid line) and the SiC data, (b) are presented after removal of the silicon background according to the procedure explained in Section 2. The spectra are shifted for clarity.

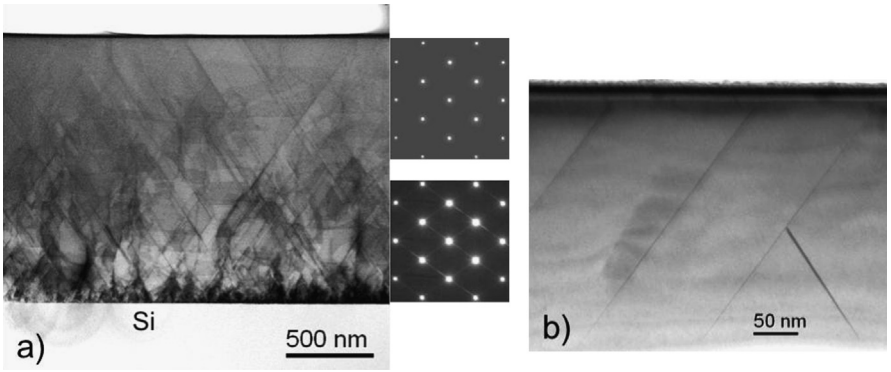

Fig. 12. (a) Low magnification STEM-HAADF image (with inverted contrast) of the SiC layer grown on buffer B. The SAED patterns on the right from bottom to top were taken at bottom and top part of the layer, respectively. The continuous streaks in the ⟨111⟩ directions in the bottom SAED suggest the presence of a high density of stacking faults on those planes in the bottom part of the layer. The absence of such streaks in the top part suggests a much reduced density of stacking defects as the layer thickness increases. This is confirmed by the TEM image of the top part of the layer in (b) taken in the two-beam diffraction contrast mode with diffraction vector g=⟨004⟩.

film. A similar comparison for the LO peak is not possible due to the uncertainties in the fitting procedure for the LO peak in the buffer, as explained previously. Considering the positions of the LO and TO peaks in the film, compared to the bulk, we can calculate a residual tensile strain of about 0.03%, a very low value considering the thickness of the film of about 1.5 μm [32]. Also the low FWHM of the LO peak is confirming the high crystal quality of the SiC film grown on the optimized buffer.

Fig. 14 compares the profiles of the forbidden TO mode for buffer layer and SiC film respectively. It is well known that the presence of asymmetry in the profile of this peak is directly related to the presence of defects [34]. Asymmetry is clearly present in both the buffer layer and the SiC film. Detailed inspection however shows that the asymmetry present in the SiC film is exactly equal to that of the buffer layer. This leads us to infer that the SiC film in itself is not bearing any additional contribution to the asymmetry, which is an indirect confirmation of its good crystallinity and low density of defects, which can be interpreted assuming that the relaxation of the mismatch strain between Si substrate and 3C–SiC film occurs almost completely in the buffer layer. In fact, the difference between the two spectra (Fig. 14 bottom panel) leads to an almost symmetric profile of the TO mode of 3C–SiC film, as confirmation of the previous speculations.

XPS analysis of the SiC film (Fig. 15) shows that C 1s and Si 2p peak positions are shifted with respect to expected 3C–SiC BE, but, as in the case of the buffer layer (Fig. 4), the peak FWHM is comparable to the photon width (0.85 eV) and the difference in binding energy is 182.3 eV, as expected for highly crystalline material. C 1s lineshape analysis (Table S1) shows a main peak at 283.38 eV related to SiC chemical bond, with a weak component at about 285 eV due to residual contamination. Si 2p core level is composed of a main Si–C peak at 101.06 eV and a component at higher binding energies related to oxidized species. The very low FWHM of the C 1s peak and the BE difference between the C 1s and Si 2p SiC peaks of 182.3 eV once again are evidence of a higlhy ordered 3C–SiC film.

Surprisingly, the standard XPS characterizations on the bulk SiC and buffer layer films lead to a stoichiometry with a variable silicon to carbon ratio of about 1.5–1.7 (± 0.08), in spite of the expected value of 1 for such a crystalline film. To check the origin of this silicon excess, XPD analysis was performed on the thick 3C–SiC. The evolution of the C 1s and Si 2p peak intensities (normalized to their sensitivity factors in order to better visualize the real stoichiometry) is characterized by strong variations (see Fig. 16), with the Si/C ratio varying from 1.0 to 2.0. This effect is typical in highly ordered structures and is due to a forward focusing effect [35], thus the calculated stoichiometry must take care of this effect. Similar results have been already found in SiC thin films characterized by high crystallinity [35], a further confirmation of the correct choice of a slow ramp procedure, which leads to an improved crystalline structure.

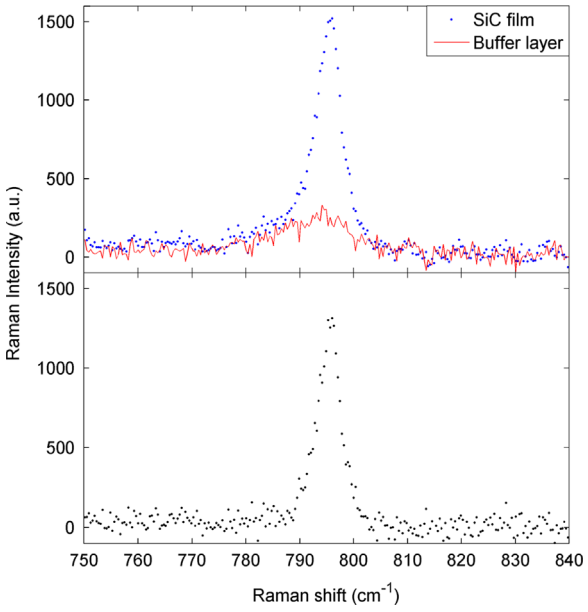

Fig. 14. Top panel: 3C–SiC TO peak of the buffer layer (red line) and the SiC film (black line). Bottom panel: difference between the two.

3.4. Discussion

During the optimization of the buffer layer the most critical parameter was the heating ramp. A fast heating ramp (25.5 °C/min), regardless of the C_3H_8 and SiH_4 flow used, resulted in a degraded

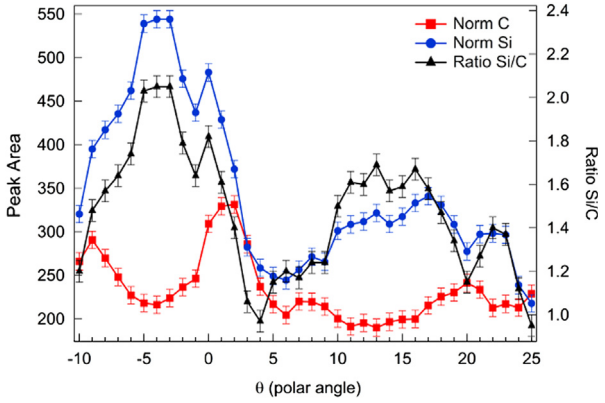

Fig. 16. XPD scan over polar angle (θ) of a bulk crystalline 3C–SiC sample grown on the best buffer SiC layer. Azimuthal angle is 0°. Si 2p and C 1s peak area are calculated subtracting a Shirley Background and are normalized to their relative sensitivity factors.

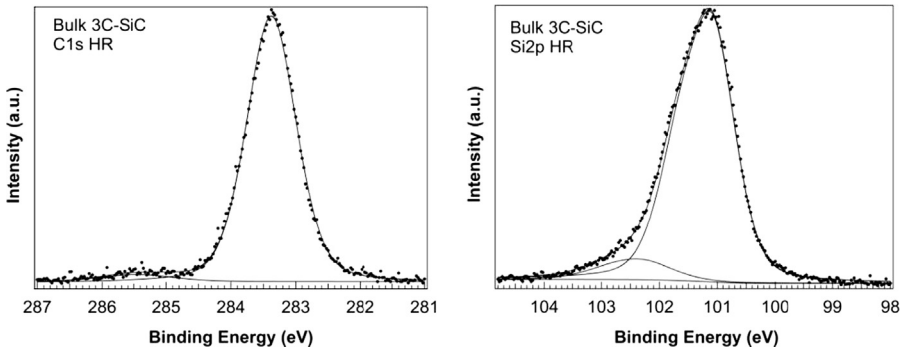

Fig. 15. High resolution XPS Spectra of bulk 3C–SiC at PE = 10 eV, background subtracted and with lineshape analysis. Left: C 1s. Right: Si 2p.

buffer, with high polycrystalline content and a high density of interface voids. The thick films grown on these buffers showed the absence of the (002) XRD reflection and an intense (111) peak, indicating the absence of epitaxial relationship with the Si substrate. TEM images of the non-optimized buffer, with evidence of polycrystalline grains with high reciprocal misorientation, suggest that the growth rate in this case is too fast to promote an ordered growth of the nuclei on the carbonized substrate. This results in an incomplete coverage, that promotes silicon outdiffusion from the Si surface and the generation of pits and voids. As a consequence an overpressure of Si could be present in the gas phase, altering the optimal Si/C conditions for the buffer growth.

A slower heating ramp (21.5 °C/min) significantly increased the crystal quality of the buffer layer and avoided the formation of interface voids. In this case small islands nucleate on the carbonized silicon substrate and undergo a progressive enlargement maintaining a flat surface. The evolution of the buffer appears very similar to the one proposed for high mismatched heterosystems such as GaN/sapphire [31].

Also, adatom mobility change during the ramp heating can have a role in controlling island nucleation size and to achieve a more complete and uniform surface coverage. By using a slower ramp the mobility should increase slower than by using the fast ramp, and this may help in obtaining a better low temperature SiC template for subsequent growth.

From our study it is also evident that the holes at the SiC/Si interface do not form during the carbonization, but preferentially during the heating stage from the carbonization to the high temperature regime for the SiC growth. The growth phase between the carbonization and the film can thus be considered one of the most important parameter to control and to optimize and, from our results, a fine tuning of the growth parameter in order to promote a slow, monocrystalline and uniform growth appears absolutely necessary.

The SiC deposited on the best buffer layer, although it can be further optimized by fine tuning the growth parameters, showed characteristics comparable to the state of the art. The XRD FWHM is very low, and there is the possibility for further improvement by increasing the film thickness, as usually reported in literature. Raman analysis suggests very low stress value, making these layers optimal candidates for MEMS processing. The surface was observed to be very flat, with evidence of atomic steps: this characteristic is considered crucial to realize graphene on 3C–SiC [5,36] or to optimize surface functionalization, e.g., for biocompatible devices or interface with organic molecules [2].

4. Conclusions

A procedure for the optimization of a 3C–SiC buffer layer for the deposition of 3C–SiC/(001) Si is presented. The growth procedure between the carbonization and the thick film deposition is found to be a very important step, often not accurately described in literature. In order to obtain a good buffer layer for the growth of high quality SiC at 1380 °C it is mandatory an accurate control of the heating ramp rate from the carbonization to the SiC growth high temperature. A slow ramp (21.5 °C/min) was found effective to eliminate the presence of typical voids at the SiC/Si interface and to obtain a good monocrystalline film with a smooth surface. In our process the interfacial pits were mostly formed during the heating ramp from the carbonization to 1380 °C if a fast ramp is used (25.5 °C/min). The gas flow rate was found to have less impact on the final result. Better results were obtained with higher gas flows, but it was necessary to progressively change the SiH_4 and C_3H_8 content in the gas phase in order to prevent precursor depletion in the growth chamber.

The high-quality of the 3C–SiC layers grown on the optimized buffer thus obtained demonstrates the effectiveness of the described buffer.

Acknowledgments

The authors are grateful to Mr. C. Mora for performing countless XRD measurements during the optimization of the buffer layer. AFM images were obtained at the “Centro Interfacoltà Misure” of Parma University. M.B. would like to acknowledge CNR for the short term mobility program to University of South Florida, Tampa, USA and Prof. S.E. Saddow and Dr. C. Locke for the time spent there and the interesting discussions on SiC growth. The films grown in this paper were deposited on Si substrates kindly provided by Dr. G. Borionetti of MEMC, Novara (Italy).

Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.jcrysgro.2013.08.005.

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